CLAIMS

The invention claimed is:

1. A method of forming circuit traces and contact pads for an interposer utilized in a semiconductor package, comprising:

providing an interposer substrate having a pair of opposing surfaces; the opposing surfaces being a first surface and a second surface; the substrate having a conductive layer over the first surface;

forming pads over the conductive layer by plating a conductive material over the conductive layer while using the conductive layer as an electrical connection to a power source; and

after the plating, patterning the conductive layer into electrical traces.

2. The method of claim 1 wherein the conductive layer extends across an entirety of the first surface.

3. The method of claim 1 wherein the forming the pads comprises plating a nickel containing layer over the conductive layer and plating a gold-containing layer physically against the nickel-containing layer.

4. The method of claim 1 wherein the conductive layer predominately comprises copper, and has a thickness of at least about 10 microns.

5. The method of claim 1 wherein the conductive layer predominately comprises copper, and has a thickness of less than or equal to about 5 microns.

6. The method of claim 1 wherein the conductive layer predominately comprises copper, and has a thickness of less than or equal to about 5 microns; the method further comprising, prior to forming the pads, forming a patterned conductive material over the conductive layer; the patterned conductive material defining a pattern of the electrical traces; and wherein the patterned conductive material is utilized as a mask during the patterning of the conductive layer into the electrical traces.

7. The method of claim 6 wherein the patterned conductive material predominately comprises copper, and has a thickness of at least about 10 microns.

8. The method of claim 1 wherein no bus lines are utilized in addition to the conductive layer during the plating.

9. The method of claim 1 wherein the conductive layer comprises copper.

10. The method of claim 1 wherein the conductive layer is a first conductive layer, and further comprising a second conductive layer extending over the second surface; and wherein the pads are formed over the first and second conductive layers during the plating.

11. A method of forming circuit traces and contact pads for an interposer utilized in a semiconductor package, comprising:

providing an interposer substrate having a surface and a conductive layer extending over the surface, the substrate having a central region where an opening will ultimately be formed to extend entirely through the substrate, and having a peripheral region extending around the central region;

forming contact pads over the conductive layer within the peripheral region by plating a conductive material over the conductive layer while using the conductive layer as an electrical connection to a power source and without utilizing conductive busses, other than the conductive layer, extending over any portion of the central region of the substrate; and

after the plating, forming the opening within the central region of the substrate and extending entirely through the substrate.

12. The method of claim 11 wherein the conductive layer extends across an entirety of the surface.

13. The method of claim 11 wherein the conductive layer has a thickness of less than about 5 microns during the plating of the conductive material.

14. The method of claim 11 wherein the conductive layer is a first conductive layer; the method further comprising forming a second conductive layer over the first conductive layer prior to the plating of the conductive material; wherein the second conductive layer is in a pattern of circuit traces; and wherein the contact pads are formed physically against the second conductive layer.

15. The method of claim 14 further comprising transferring the pattern of the second conductive layer to the first conductive layer after the plating of the conductive material.

16. The method of claim 11 wherein the conductive layer has a thickness of greater than about 10 microns during the plating of the conductive material.

17. The method of claim 11 wherein the semiconductor package is a board-on-chip construction.

18. A method of forming circuit traces and contact pads for an interposer utilized in a semiconductor package, comprising:

providing an interposer substrate having a pair of opposing surfaces; the opposing surfaces being a first surface and a second surface; the substrate having a first conductive layer over the first surface;

forming a second conductive layer over and in physical contact with at least portions of the first conductive layer;

forming a patterned mask to cover portions of the second conductive layer while leaving other portions exposed through openings in the mask;

plating a third conductive layer over the exposed portions of the second conductive layer while using the first conductive layer as an electrical connection between the exposed portions and a power source; and

after the plating, patterning the first conductive layer into electrical traces.

19. The method of claim 18 wherein the first conductive layer comprises copper.

20. The method of claim 18 wherein the first and second conductive layers comprise copper.

21. The method of claim 18 wherein the third conductive layer comprises one or more of nickel, gold and palladium.

22. The method of claim 18 wherein the semiconductor package is a board-on-chip construction.

23. A method of forming circuit traces and contact pads for an interposer utilized in a semiconductor package, comprising:

providing an interposer substrate having a pair of opposing surfaces; the opposing surfaces being a first surface and a second surface; the substrate having a first conductive layer over the first surface;

forming a first patterned mask over the first conductive layer; the first patterned mask having openings extending therethrough to the first conductive layer; the openings defining a circuit pattern;

forming a second conductive layer over and in physical contact with portions of the first conductive layer exposed through the openings; the second conductive layer thereby being formed in the circuit pattern;

forming a second patterned mask to cover portions of the second conductive layer while leaving other portions exposed through openings in the second patterned mask; the exposed portions of the second conductive layer being contact pad locations;

plating a third conductive layer over the contact pad locations while using the first conductive layer as an electrical connection to a power source;

removing the first and second patterned masks; and

patterning the first conductive layer into electrical traces defined by the circuit pattern of the second conductive layer.

24. The method of claim 23 wherein the first conductive layer predominately comprises copper, and has a thickness of less than or equal to about 5 microns.

25. The method of claim 23 wherein the first conductive layer predominately comprises copper and initially has a first thickness greater than about 10 microns, the method further comprising reducing a thickness of the first conductive layer to less than or equal to about 5 microns prior to forming the second conductive layer.

26. The method of claim 23 wherein the second conductive layer and first conductive layer predominately comprise copper, and wherein a combined thickness of the first and second conductive layers is greater than about 10 microns.

27. The method of claim 23 wherein the third conductive layer comprises nickel, and further comprising forming a layer comprising gold over the third conductive layer prior to removing the first and second patterned masks.

28. The method of claim 23 further comprising forming an opening extending entirely through the substrate after plating the third conductive layer.

29. The method of claim 23 wherein the semiconductor package is a board-on-chip construction.

30. The method of claim 29 wherein:

a fourth conductive layer is over the second surface;

a third patterned mask is formed over the fourth conductive layer, and the third patterned mask has openings extending therethrough to the fourth conductive layer;

the second conductive layer is formed within the openings in the third patterned mask during the forming of the second conductive layer over and in physical contact with the first conductive layer;

after the second conductive layer is formed, a fourth patterned mask is formed over the fourth conductive layer to protect regions of the fourth conductive layer which are to be formed into circuit traces while leaving other portions of the fourth conductive layer exposed; and

the fourth conductive layer is patterned into circuit traces during the patterning of the first conductive layer into circuit traces.

31. A method of forming circuit traces and contact pads for an interposer utilized in a semiconductor package, comprising:

providing an interposer substrate having a pair of opposing surfaces; the opposing surfaces being a first surface and a second surface; the substrate having a first conductive layer over the first surface;

forming a first patterned mask over the first conductive layer; the first patterned mask having openings extending therethrough to the first conductive layer; the openings defining contact pad locations;

forming a second conductive layer over and in physical contact with portions of the first conductive layer exposed through the openings; the second conductive layer thereby being formed at the contact pad locations;

removing the first patterned mask;

forming a second patterned mask over the first conductive layer; the second patterned mask protecting regions of the first conductive layer while exposing other regions; the protected regions defining circuit traces to at least some of the contact pad locations;

removing unprotected regions of the first conductive layer to form the circuit traces from the first conductive layer; and

removing the second patterned mask.

32. The method of claim 31 wherein the semiconductor package is a board-on-chip construction.

33. A method of forming circuit traces and contact pads for an interposer utilized in a semiconductor package, comprising:

providing an interposer substrate having a pair of opposing surfaces; the opposing surfaces being a first surface and a second surface; the substrate having a first conductive layer over the first surface and a second conductive layer over the second surface;

forming a first patterned mask over the first and second conductive layers; the first patterned mask having openings extending therethrough to the first and second conductive layers; the openings defining contact pad locations;

forming a third conductive layer over and in physical contact with portions of the first and second conductive layers exposed through the openings; the third conductive layer thereby being formed at the contact pad locations;

removing the first patterned mask;

forming a second patterned mask over the first and second conductive layers; the second patterned mask protecting regions of the first and second conductive layers while exposing other regions; the protected regions defining circuit traces to at least some of the contact pad locations;

removing unprotected regions of the first and second conductive layers to form the circuit traces from the first and second conductive layers; and

removing the second patterned mask.

34. The method of claim 33 wherein the first and second conductive layers predominately comprise copper, and have thicknesses of greater than or equal to about 10 microns.

35. The method of claim 33 wherein the third conductive layer is formed by plating while using the first and second conductive layers as electrical interconnects to a power source.

36. The method of claim 33 wherein the third conductive layer comprises nickel, and further comprising forming a layer comprising gold nickel over the third conductive layer in the contact pad locations.

37. The method of claim 33 further comprising forming an opening extending entirely through the substrate after forming the circuit traces from the first and second conductive layers.

38. The method of claim 33 further comprising forming an opening extending entirely through the substrate and subsequently providing a conductive material within the opening to electrically connect the first and second conductive layers.

39. The method of claim 38 wherein the opening is formed before forming the first patterned mask.